Product ID: 2214

ITDev FPGA IP Core Product Brief

SDR/HDR Colour Space Converter

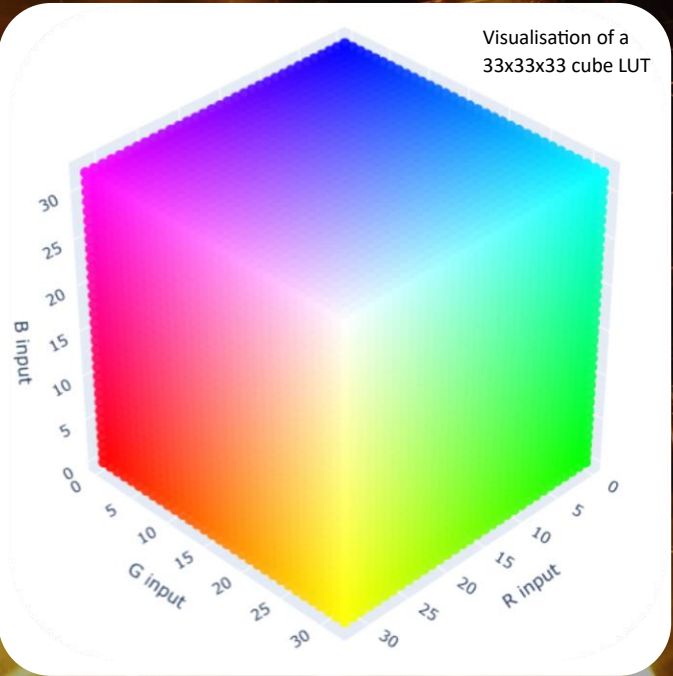
This IP core performs the operations necessary to convert between SDR video and HDR video in either direction. The core can be loaded with industry recognised LUTs (look-up tables) to perform colour conversion between standards such as BT.709, BT.2100 & BT.2020. Optionally reconfigurable via AMBA® 4 AXI-Lite, the core can also be used to optimise colours within a video pipeline for broadcast monitors, projection systems, medical displays, AV over IP, etc.

Features

- Supports all common formats including 4Kp60
- Less than one line of latency
- Tetrahedral interpolation
- Configurable LUT size
- Works in AMD Vivado™ IP Integrator
- Uses AMBA 4 AXI-Stream Video

Optional extensions include:

- Pre/post colour space conversion tone correction LUTs
- AMBA 4 AXI-Lite LUT reprogramming on the fly



Visualisation of a 33x33x33 cube LUT

Benefits

Easy to integrate using either RTL or AMD's block design flow, this highly configurable core delivers maximum functionality for minimum integration effort. Its tetrahedral interpolation provides faithful conversion resulting in high image quality. The core has been optimised for resource utilisation and timing closure, not only through efficient implementation but also through a carefully considered pipeline architecture.

Demo

A demonstration is available showing this IP up-mapping SDR content to HDR. This runs on a ZCU104 Zynq™ development board and uses AMD's HDMI 2.0 core to receive 4K60 input in RGB 24-bit format and output RGB in 30-bit.

In addition to the above, a downloadable demo for the Kria™ platform will be available soon.

Deliverables

The following items are included in the delivery package:

- Encrypted RTL source code
- AMD IP Integration package
- Delivery testbench showing operation of conversion IP

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Resource Utilisation Guide

Pixels In Parallel	Input Bit Depth	Output Bit Depth	3D LUT Size	LUT Width	RAMB36E	CLB LUTs	CLB Register
2	8	10	17^3	10	15	5788	5837
2	8	10	33^3	10	39	4700	4558
2	8	10	65^3	10	292.5	3800	3545
4	8	10	17^3	10	30	11602	11669
4	8	10	33^3	10	78	6976	5927
2	10	10	33^3	10	39	7010	7239

- Spartan™ 7 FPGAs, Artix™ 7 FPGAs
  100MHz target clock (74.25MHz required for 1080p60 @ 2PPC over SDI)
- Kintex™ 7/Ultrascale™/Ultrascale+™ FPGAs, Zynq™ Ultrascale+ MPSoC, and Artix Ultrascale+ FPGAs
  300MHz target clock (297MHz required for 2160p60 @ 2PPC over SDI)

Performance subject to individual use-case and FPGA utilisation, congestion, and speed grade.
The symbol "^{3}" refers to the LUT being a cube. For example, a 17^3 LUT consists of 17x17x17 values.

Video Formats

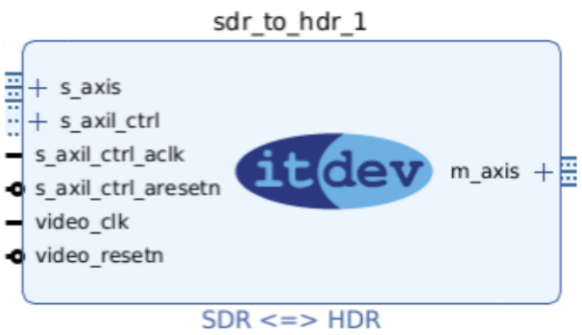
Operations are performed at a pixel level, so image size and frame rate determine the necessary clock speed of the IP. The utilisation figures above are based on a clock speed of 300MHz, which is sufficient to handle 4K at 60 fps with a single instance. If a clock rate sufficient for a larger size or higher frame rate cannot be achieved, multiple instances of this block may be used in parallel.

About ITDev

Formed in 2000, ITDev have been developing FPGA video solutions for more than 15 years. Having operated in a range of markets including pro AV, broadcast, aerospace, security and healthcare, we're well placed to provide integration support, or even full product development.

You can find more information, including testimonials on our website at www.itdev.co.uk.

Example of block diagram interfaces



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