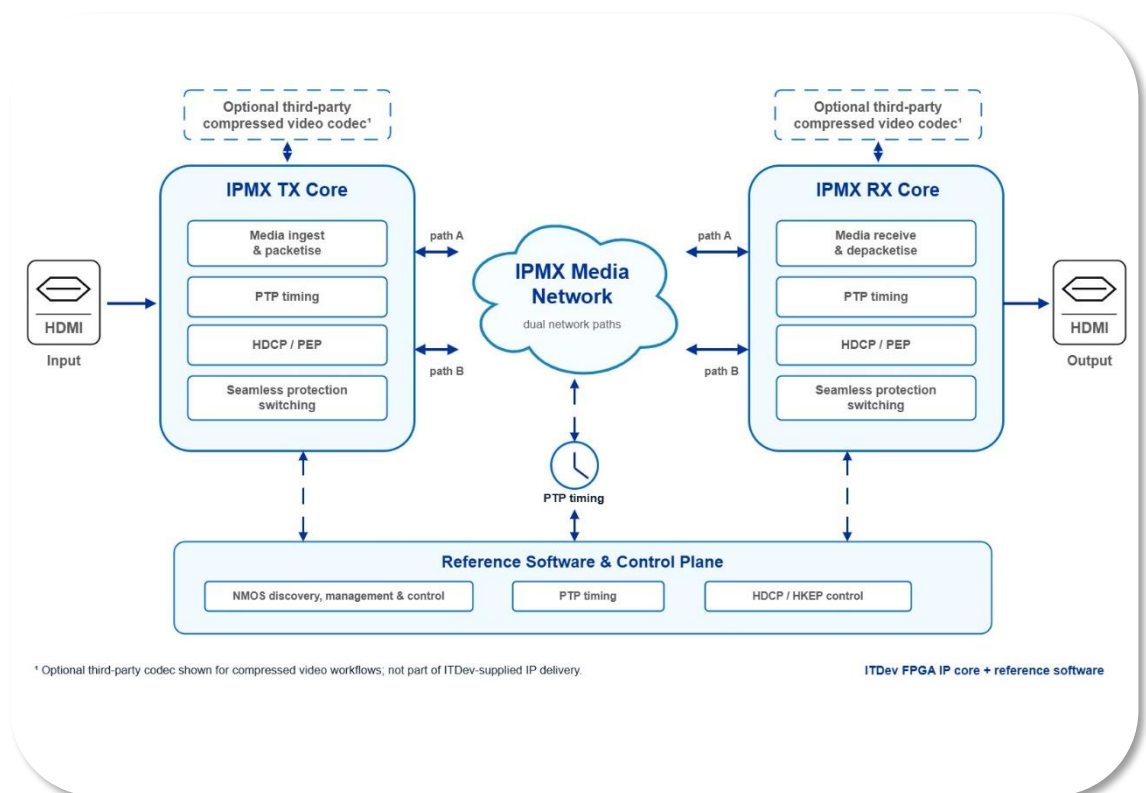


FPGA IP Core for IPMX Products

Product Brief

Accelerate IPMX product development with a single FPGA IP core designed for open, standards-based AV-over-IP products. Based on the VSF TR-10 suite of standards, the core supports uncompressed video and optional compressed video workflows, PTP timing, NMOS discovery, management and control, and scalable network operation from 1G to 100G. HDCP/HKEP and PEP support is forthcoming.



- Uncompressed & Compressed Video**
- Synchronous & Asynchronous Video
- Precision Time Protocol
- NMOS Discovery, Management & Control
- HDCP Protection**
- Seamless Protection Switching
- Uncompressed & Compressed Audio
- Offers sub-frame latency

*RX only **Coming Soon

COMPATIBILITY

VSF TR-10

AMWA NMOS

SMPTE ST 2110

SMPTE ST 2059

SMPTE ST 2022-7

APPLICATIONS

Broadcast & Media

Corporate

Education

Healthcare

Public Sector

Retail & Hospitality

SPECIFICATIONS

TX & RX

HD – 4K+ resolutions

RGB, YCbCr 4:4:4 & 4:2:2

8, 10, 12-bit* colour depths

1G, 10G, 25G, 100G networks

Standards Compatibility

VSF TR-10-1	System Timing / Precision Time Protocol (PTP)
VSF TR-10-2	Uncompressed Active Video
VSF TR-10-3	PCM Digital Audio
VSF TR-10-5	HDCP Key Exchange Protocol**
VSF TR-10-6	Forward Error Correction (FEC)**
VSF TR-10-8	NMOS Requirements
VSF TR-10-9	System Environment and Device Behaviour
VSF TR-10-11	Constant Bit-Rate Compressed Video**
VSF TR-10-12	AES3 Transparent Transport
VSF TR-10-13	Privacy Encryption Protocol (PEP)**
ST 2022-7	Seamless Protection Switching
ST 2110	-10, -20, -21, -22, -30, -31
ST 2059	-1, -2 PTP Timing Environments
NMOS	IS-04, IS-05 & IS-11, BCP-004-01, BCP-004-02

*RX only **Coming Soon

Deliverables

IP Delivery	Encrypted Netlist & Supporting Software AMD IP integration package Product guide
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Reference Design

Streamline IPMX product development with ITDev reference designs for the AMD Zynq™ Ultrascale+™ ZCU106 MPSoC reference platform, demonstrating HDMI I/O and network operation up to 10G.

AMD
together we advance_

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sales@itdev.co.uk

www.itdev.co.uk

+44 (0)23 8098 8890

IP Reference # 2406

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